

VHDL Implementation of $\pi/4$ QPSK MODEM

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ABSTRACT

$\pi/4$ QPSK technique is one of the most popular Phase shift keying technique used widely in wireless communication systems like satellite radio. Using analog circuits to implement the modulator and demodulator is not suitable for some applications like biomedical signal transmission. Analog circuits have large size and high power consumption. So for such application we have to go for digital methods of implementation. The main advantages of the digital design are frequency agility, repeatability, cost and the simpler reconfiguration compared to analog. Very high speed integrated circuits hardware description language (VHDL) enables us to model a digital system. This system then can be physically implemented on hardware using field programmable gate arrays (FPGA), which is a highly configurable silicon engine. In this paper $\pi/4$ QPSK modulator and demodulator (MODEM) is designed in VHDL and its expected simulation is carried on Xilinx ISE 8.2i environment.

Keywords:- PSK, QPSK, VHDL, FPGA, MODEM

I. INTRODUCTION

The modulator and demodulator are the basic building blocks of a communication system. They are designed in such way that the channel distortion is as minimum as possible. There are many types of modulation techniques, out of which Phase shift keying (PSK) is one. In PSK we vary the phase of carrier signal in accordance with the baseband signal. Quadrature phase shift keying (QPSK) is one of the PSK technique in which four different states or carriers are used to represent a group of two bits input data. QPSK is used to achieve higher data rate which is double than that of Binary phase shift keying (BPSK) [1].

QPSK is a part of signals called constant envelope signal. These are special signals whose amplitude after sampling is constant. This signals suffers less distortion in high power amplifier. So we can use them for wireless application [2]. But the major drawback that simple QPSK system has is its 180° envelope variation. Because of this amplifiers leads to distortion as sudden change in amplitude takes place. This disadvantage of simple QPSK is overcome in $\pi/4$ QPSK technique.

$\pi/4$ QPSK system is one which like simple QPSK transmits two bits per symbol. In QPSK we have four signals that are used to transmit four two bit symbols. In $\pi/4$ QPSK we have eight signals. Every alternate symbol is transmitted using a $\pi/4$ shifted pattern of QPSK constellation [3]. It uses two identical constellations which are rotated by 45° with respect to one another, which is shown in fig. 1. Usually, either the even or odd

symbols are used to select points from one of the constellations or the other symbols select points from the other constellation.

So we get a phase shift of $\pi/4$ between two symbols which are exactly identical [4].

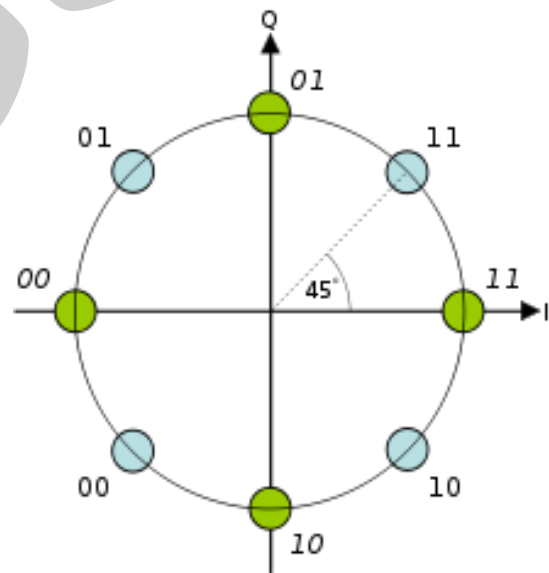


Fig. 1 Dual Constellation Diagram for $\pi/4$ -QPSK

So $\pi/4$ QPSK technique is much suitable than QPSK as it preserves the property of constant envelope signal. The 180°

envelope variation which was one of the major drawback of simple QPSK system is now reduced to just 135° in case of $\pi/4$

Differentially detected [5]. Also as the set of constellation points changes each symbol, so transition through zero never occurs. Fig. 2 shows the timing diagram for a $\pi/4$ QPSK system. It is clear from figure that envelope variation is not 180° .

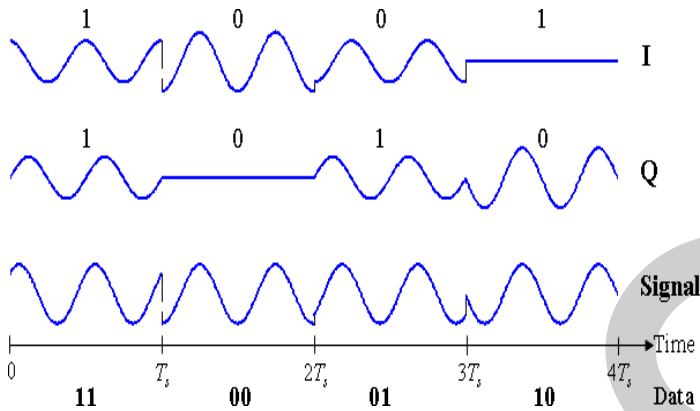


Fig. 2 Timing Diagram for $\pi/4$ -QPSK

In this paper the MODEM is designed using VHDL language. Each block of the system is modeled and combined using behavioral modeling style. The functionality of the system is checked in Xilinx ISE 8.2i environment.

II. $\pi/4$ QPSK MODULATOR

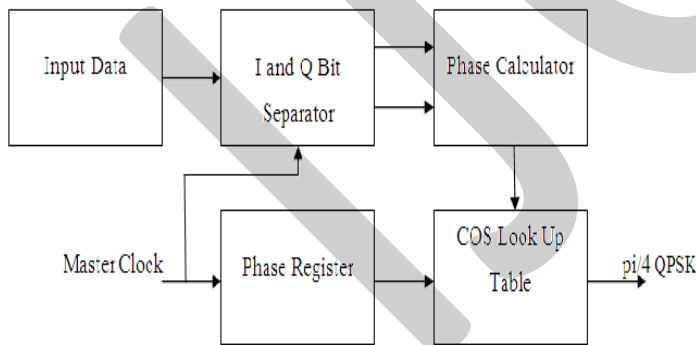


Fig. 3 $\pi/4$ QPSK Modulator

Fig. 3 shows the proposed $\pi/4$ QPSK modulator. The first block generates input data which is nothing but the digital bits. This bits are then separated into I bits and Q bits. Thus the serial bit data is now converted into parallel bit streams. Phase

calculator block calculates the phase shift between the incoming bits. Phase register gives us the value for instantaneous phase. Cos LUT has phase versus amplitude table stored in RAM. Depending on the values of this look up table Cos LUT map the bits into $\pi/4$ QPSK signal. Master clock is there for synchronization of all the blocks.

calculator block calculates the phase shift between the incoming bits. Phase register gives us the value for instantaneous phase. Cos LUT has phase versus amplitude table stored in RAM. Depending on the values of this look up table Cos LUT map the bits into $\pi/4$ QPSK signal. Master clock is there for synchronization of all the blocks.

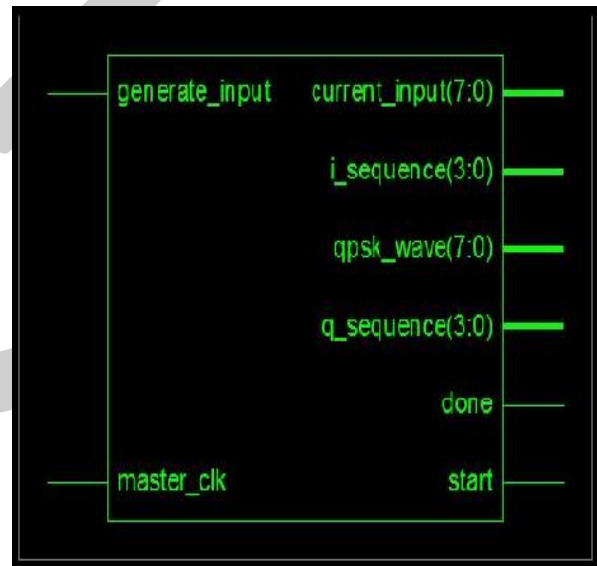


Fig. 4 RTL view of $\pi/4$ QPSK Modulator

The VHDL modulator as shown in fig. 4 will take generate input and master clock as its inputs. The output of modulator consists of I sequence, Q sequence and QPSK wave. Start and Done signals indicate the starting of modulation and ending of modulation. The RTL schematic view of modulator is shown in fig. 5.



Fig. 5 RTL schematic view of $\pi/4$ QPSK Modulator

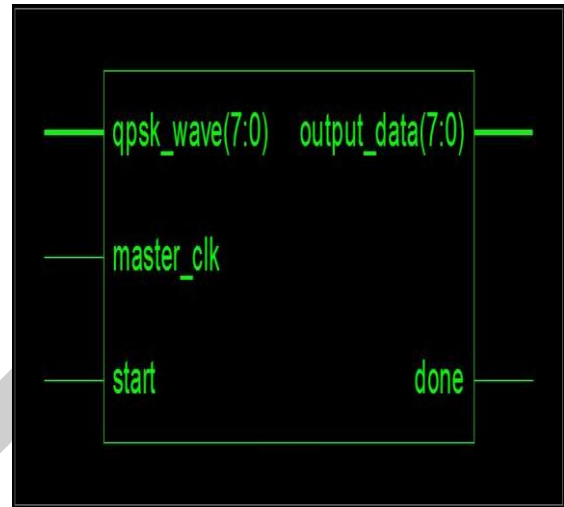


Fig. 7 RTL view of $\pi/4$ QPSK Modulator

III. $\pi/4$ QPSK DEMODULATOR

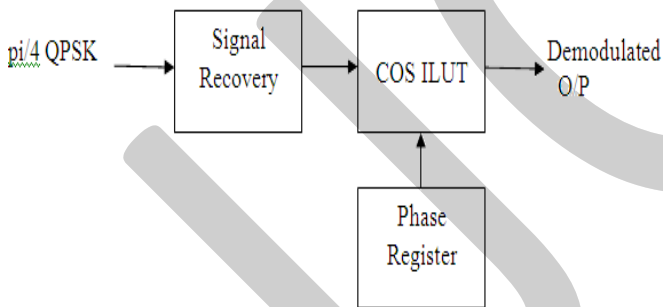


Fig. 6 $\pi/4$ QPSK Demodulator

Fig. 6 shows the $\pi/4$ QPSK demodulator. It consists of a signal recovery unit the output of which is given to the Cos ILUT block. This block does the inverse function than that of Cos LUT. It will map the modulated signal into the original data with the help of phase register. The output of Cos ILUT block gives us the demodulated data.

IV. $\pi/4$ QPSK MODEM

The system consists of modulator as well as demodulator which is designed by combining these two blocks. VHDL has the facility of implementing each block of a system individually by writing its code separately. This blocks then can be joined together to form a system. This minimizes errors to a great extent. Fig. 8 shows the RTL view of $\pi/4$ QPSK MODEM.

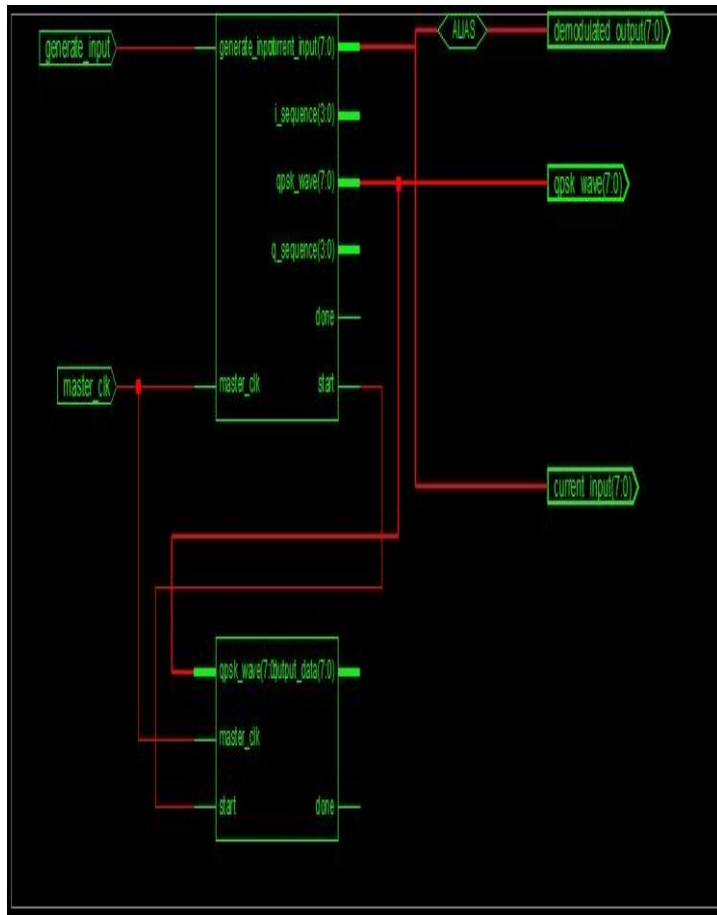


Fig. 8 RTL Schematic view of $\pi/4$ QPSK MODEM

V. SIMULATION RESULTS

The simulation for modulator block is shown in fig. 9. The modulation is done for eight bit data. We are getting I sequence and Q sequence at the output. The $\pi/4$ QPSK signal depends on the value of I and Q bits. The simulation result for complete system or MODEM is shown in fig. 10. We are getting the same output which we are giving as input. In this way we are performing modulation as well as demodulation by using one single system.

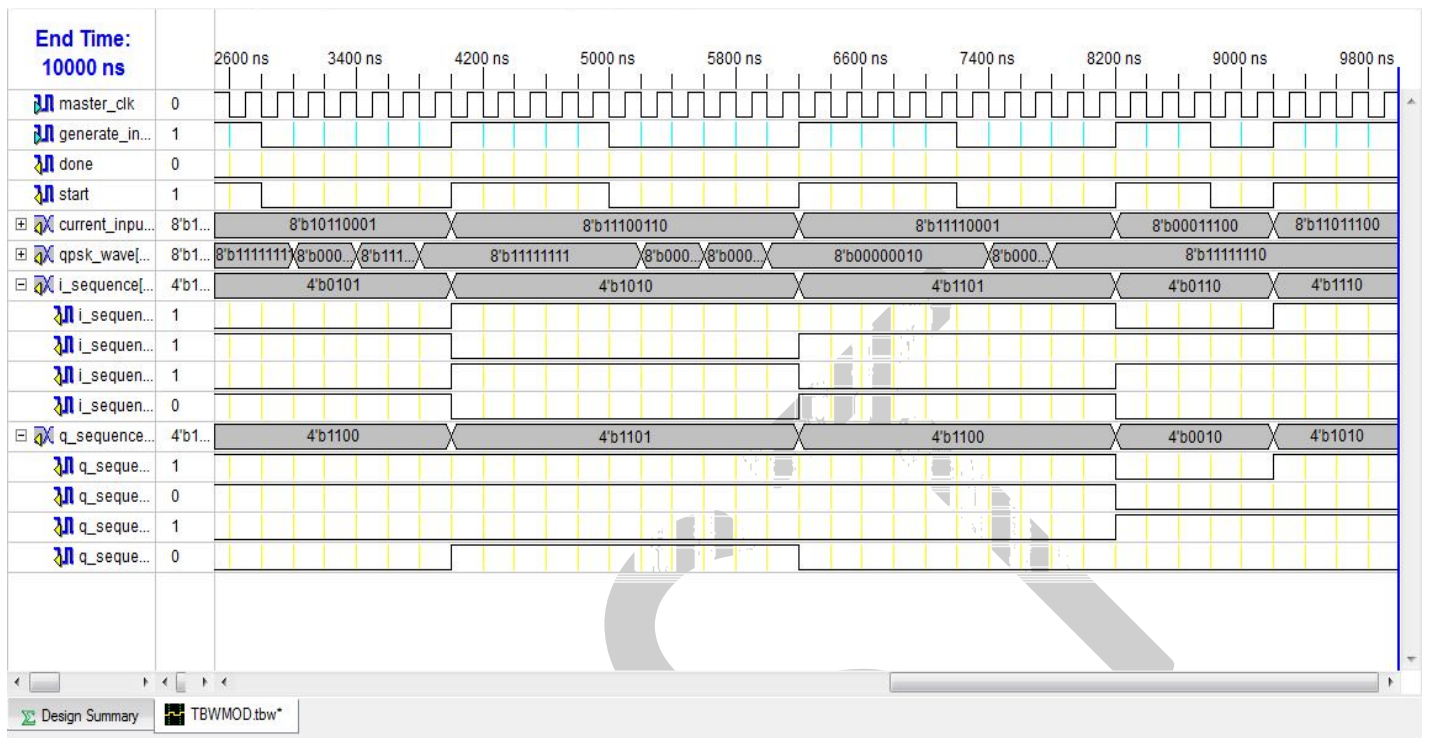


Fig. 9 Simulation result of $\pi/4$ QPSK Modulator

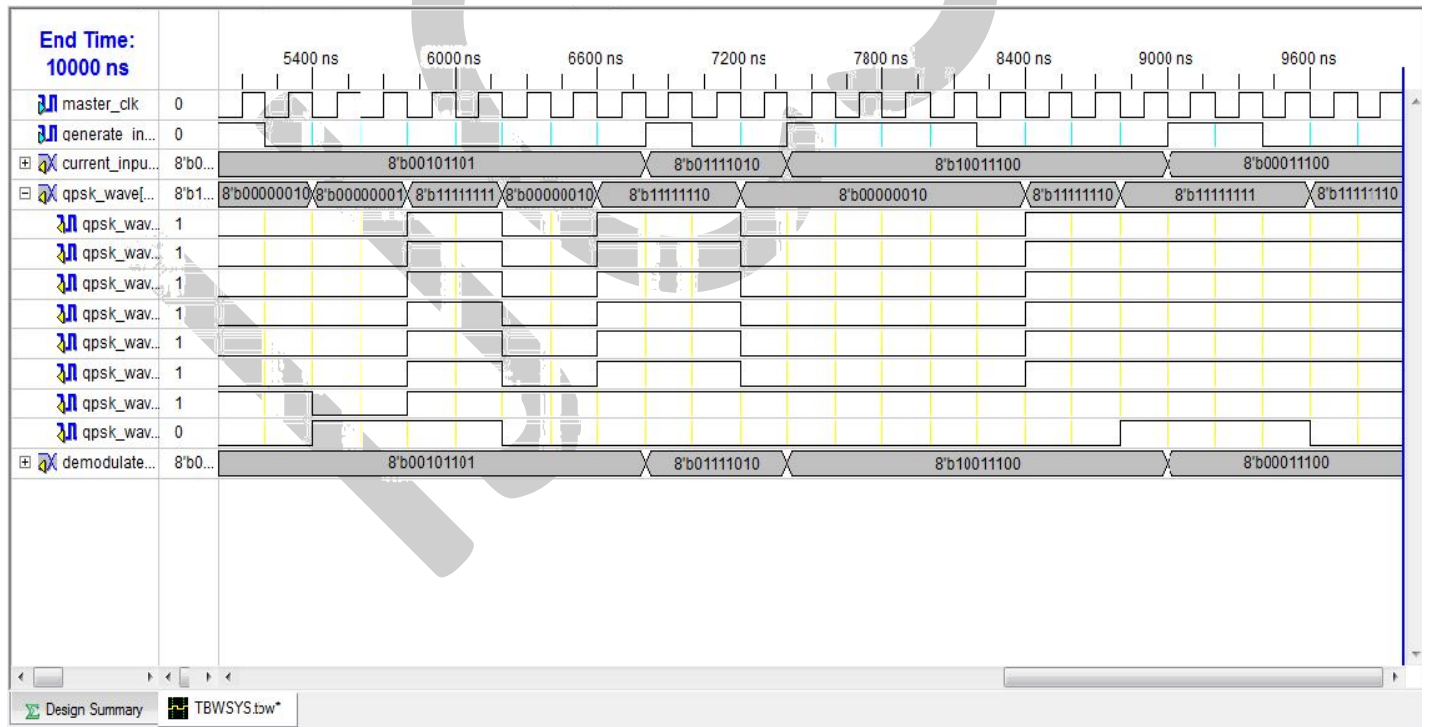


Fig. 10 Simulation result for $\pi/4$ QPSK MODEM

VI. CONCLUSION

In this paper we have designed PI/4 QPSK system on VHDL and simulation is done using Xilinx ISE environment. The system can be implemented on FPGA kit. As the system can be designed is using only digital circuits the size of this system will be small as compare to conventional system. The power consumption will also be very less. These features will make it suitable for biomedical application.

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