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A Low Power High Speed Double Tail Comparator in 90nm CMOS Technology

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ABSTRACT
Comparator is an important element in many Data converter circuits, Signal processing systems, such as telecommunication interfaces and in the sensory circuits. Also comparators are the basic building elements for designing modern analog and mixed signal systems. Many high speed analog to digital converters, such as Flash ADCs, require low power, high speed comparators with small chip area. In this paper, a novel new double tail comparator which consumes very less power and can operate at high speeds when compared to the existing double tail comparators is proposed and simulated. Because of its high speed and low power consumption it can be used in high speed analog to digital converters, such as Flash ADCs requiring low power, high speed comparators. The designed double tail comparator is simulated using HSPICE tool with 90nm technology. From the simulation results, it is observed that in the proposed double tail comparator both the power consumption and delay time are significantly reduced.

Keywords:- Double-tail comparator, Clocked Regenerative Comparator, Positive feedback, Switching transistor.

I. INTRODUCTION

One of the most important basic building blocks in analog and mixed-mode circuits is the comparator. The function of a CMOS comparator is to compare an input signal with a reference signal and produce a binary signal output. Comparator uses back to back cross coupled inverters to convert the voltage into digital output in a short period of time. The performance of the comparator plays an important role in realization of high integration, low power, low cost and good design.

Designing high-speed comparators is more challenging when the supply voltage becomes smaller [2]. In other words, in a given technology, to achieve high speed, larger transistors are required to compensate for the reduced supply voltage. It also means that more die area and power is needed. Besides, low-voltage operation results in limited common-mode input range, which is important in many high-speed ADC architectures, such as Flash ADCs.

Clocked regenerative comparators have found wide applications in many high-speed analog to digital convertors (ADCs) because of their fast decisions due to the strong positive feedback in the regenerative latch. The recent comprehensive analyses investigate the performance of these comparators from different aspects, such as noise, offset, random decision errors and kick-back noise [5].

The rest of the paper is organised as follows. Overview of the conventional dynamic comparator, conventional double tail comparator and the modified double tail comparator are explained in SECTION II, SECTION III and SECTION IV. The proposed double tail comparator is explained in SECTION V. The simulation results and performance comparison are given in SECTION VI and SECTION VII.

II. CONVENTIONAL DYNAMIC COMPARATOR

Conventional dynamic comparator is widely used in A/D converters. The comparator has high input impedance, rail-to-rail output swing, and has no static power consumption. The schematic diagram of the conventional dynamic comparator is shown in fig 1.

The operation of the conventional dynamic comparator is explained below.

During the reset phase when CLK = 0 and M_{tail} is off, the reset transistors M_7 and M_8 pull both the output nodes Outn, Outp to V_{DD} to define a start condition and to have a valid logical level during the reset.

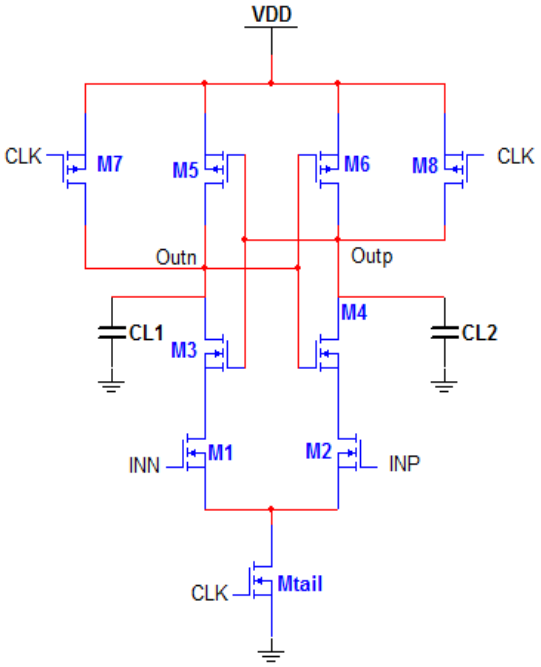

Fig. 1. Conventional dynamic comparator

In the comparison phase, when CLK = V_{DD}, transistors M_7, M_8 are off and M_{tail} is on. Output nodes (Outp, Outn) which had been pre-charged to V_{DD}, start to discharge at different discharging rates depending on the corresponding input voltages (V_{INP},V_{INN}). Assuming the case where $V_{INP} > V_{INN}$, the output node Outp discharges faster than Outn, hence with Outp (discharged by transistor M_2 drain current), falling down to $V_{DD}-|V_{thp}|$ before Outn (discharged by transistor M_1 drain current), the corresponding PMOS transistor (M_5) will turn on to initiate the latch regeneration caused by back-to-back inverters (M_3-M_5 and M_4-M_6). Thus, the output node Outn pulls to V_{DD} and Outp discharges to ground. If the input voltage V_{INP} is less than V_{INN}, the circuit works vice versa.

III. CONVENTIONAL DOUBLE TAIL COMPARATOR

The schematic of conventional double tail comparator is shown in the fig 2. This structure has less stacking and therefore can operate at lower supply voltages compared to the conventional dynamic comparator.

The double tail enables both a large current in the latching stage and wider Mtail2, for fast latching independent of the input common-mode voltage (V_{cm}), and a small current in the input stage (small Mtail1), for low offset.

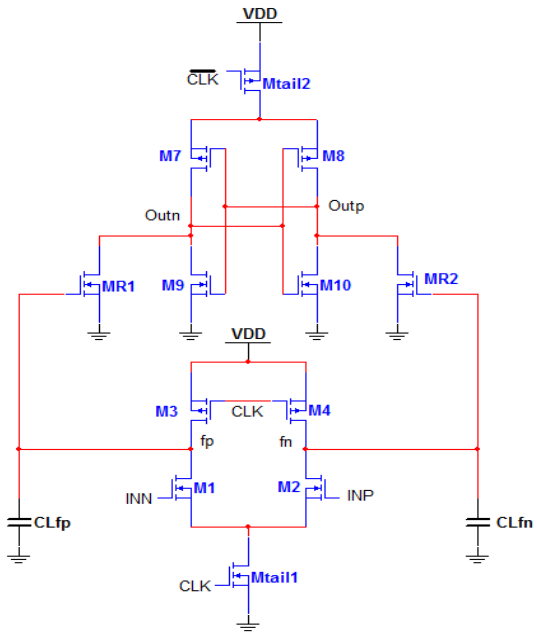

Fig. 2. Conventional double tail comparator

The operation of the conventional double tail comparator is as follows.

During the reset phase (CLK = 0, M_{tail1} and M_{tail2} are off), transistors M_3,M_4 pre-charge the nodes fn and fp to V_{DD}, which in turn make M_{R1} and M_{R2} to discharge the output nodes Outn and Outp to the ground.

During decision-making phase (CLK = V_{DD}, M_{tail1} and M_{tail2} turn on), the transistors M_3,M_4 turn off and the voltages at nodes fn, fp start to drop with the rate defined by $I_{Mtail1/Cfn(p)}$ and an input-dependent differential voltage ΔVfn(p) will also build up. The intermediate stage formed by the transistors M_{R1} and M_{R2} passes ΔVfn(p) to the cross coupled inverters and provides a good shielding between to input and output to get a reduced value of kickback noise.

IV. MODIFIED DOUBLE TAIL COMPARATOR

Fig.3 shows the schematic diagram of the modified double tail comparator. The modified double tail comparator is designed based on the double tail architecture.

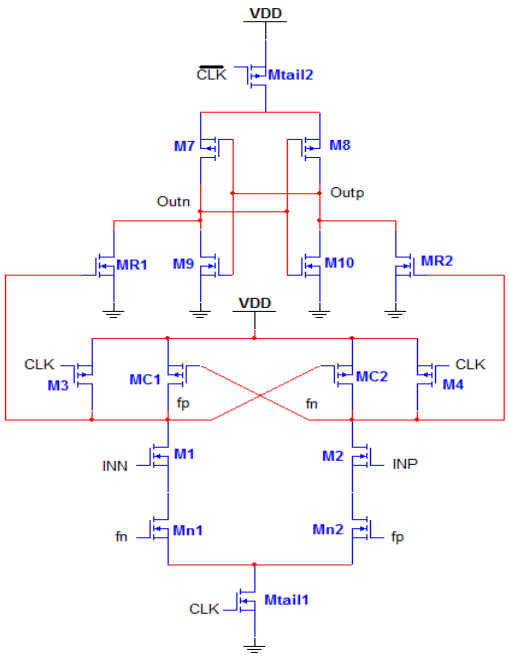

Fig. 3. Modified double tail comparator

The idea of this comparator is to increase $\Delta V_{fn/fp}$ in order to increase the latch regeneration speed. For this purpose, Mc1 and Mc2 are the two control transistors that have been added to the first stage in parallel to M_3/M_4 transistors but in a cross-coupled manner [3].

The operation of the modified double tail comparator is as follows. During reset phase (CLK = 0, M_{tail1} and M_{tail2} are off, avoiding static power), M_3 and M_4 pulls both f_n and f_p nodes to V_{DD}, hence transistor M_{c1} and M_{c2} are cut off. Intermediate stage transistors, M_{R1} and M_{R2}, reset both latch outputs to ground.

During decision-making phase (CLK = V_{DD}, M_{tail1}, and M_{tail2} are on), transistors M_3 and M_4 turn off. Furthermore, at the beginning of this phase, the control transistors are still off (since f_n and f_p are about V_{DD}). Thus, f_n and f_p start to drop with different rates according to the input voltages. Suppose $V_{INP} > V_{INN}$, thus f_n drops faster than f_p, (since M_2 provides more current than M_1). As long as f_n continues falling, the corresponding PMOS control transistor (M_{c1} in this case) starts to turn on, pulling f_p node back to the V_{DD}; so another control transistor (M_{c2}) remains off, allowing fn to be discharged completely. In other words, unlike conventional double-tail dynamic comparator, in which $\Delta V_{fn/fp}$ is just a function of input transistor trans conductance and input voltage difference, in the existing double tail structure as soon as the comparator detects that for instance node f_n discharges faster, a PMOS transistor (M_{c1}) turns on, pulling the other node f_p back to the V_{DD}. Therefore by the time passing, the difference between f_n and f_p ($\Delta V_{fn/fp}$) increases in an exponential manner, leading to the reduction of latch regeneration time.

V. PROPOSED DOUBLE TAIL COMPARATOR

Fig.4 shows the schematic diagram of the proposed double tail comparator. The proposed double tail comparator is designed based on the existing double tail architecture due to its better performance in the low voltage applications.

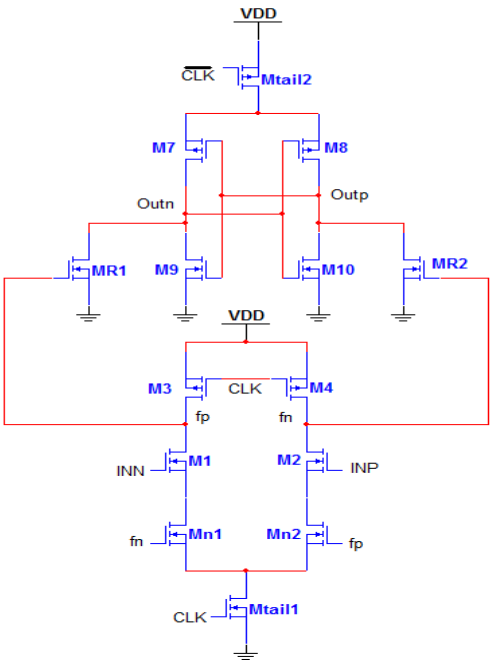

Fig. 4. Proposed double tail comparator

The idea of this comparator is to reduce the total power consumption of the circuit. For this purpose, M_{n1} and M_{n2} are the two switching transistors that have been added to the second stage in series to M_1/M_2 transistors.

The operation of the proposed double tail comparator is as follows. During the reset phase (CLK = 0, M_{tail1} and M_{tail2} are off, avoiding static power), M_3 and M_4 pulls both f_n and f_p nodes to V_{DD}. Intermediate stage transistors, M_{R1} and M_{R2}, reset both latch outputs to ground.

During decision-making phase when CLK = V_{DD}, M_{tail1}, and M_{tail2} are on and transistors M_3 and M_4 are turned off, since f_n and f_p are about V_{DD}. Thus, the nodes fn and fp start to drop with different rates according to the input voltages. Suppose if $V_{INP} > V_{INN}$, thus f_n drops faster than f_p, (since M_2 provides more current than M_1). As long as f_n continues falling, the corresponding PMOS transistor (M_3 in this case) starts to turn on, pulling f_p node back to the V_{DD}; so another transistor (M_4) remains off, allowing f_n to be discharged completely. In other words, unlike the conventional double-

tail dynamic comparator, in which $\Delta V_{fn/fp}$ is just a function of input transistor transconductance and input voltage difference, in the proposed double tail structure as soon as the comparator detects that for instance node f_n discharges faster, the PMOS transistor (M_3) turns on, pulling the other node f_p back to the V_{DD}. Therefore by the time passing, the difference between f_n and f_p ($\Delta V_{fn/fp}$) increases in an exponential manner, reducing the latch regeneration time.

With this structure, the average power consumption of the circuit is reduced when compared to the existing double tail comparator.

VI. SIMULATION RESULTS

The proposed circuit was simulated using HSPICE tool with 90nm technology. The supply voltage used in simulation is 0.8 volt. The waveforms of all the comparators are shown below.

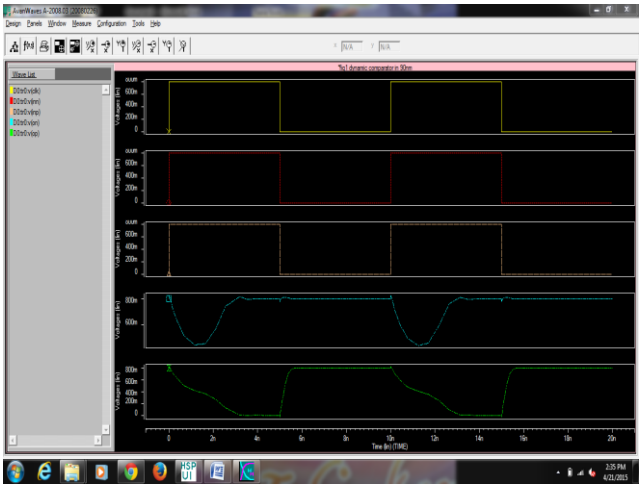

Fig. 5. Waveforms of Conventional Dynamic Comparator

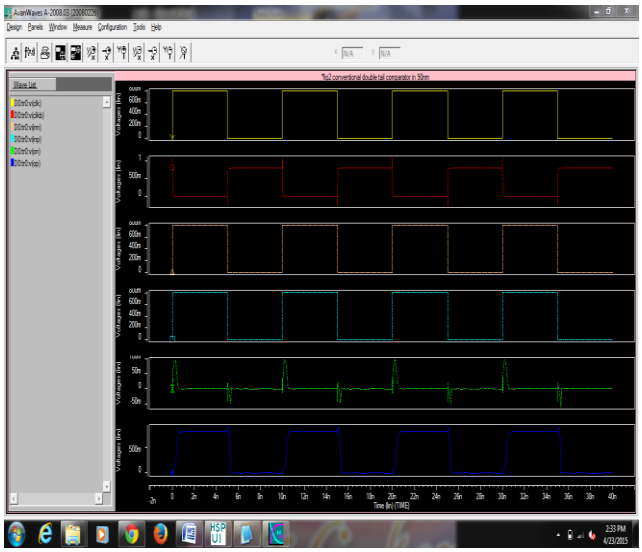

Fig. 6. Waveforms of Conventional double tail comparator

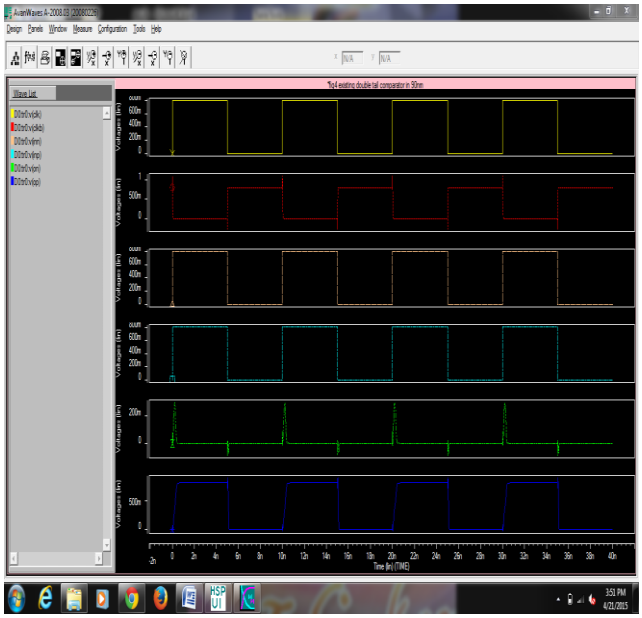

Fig. 7. Waveforms of Modified double tail comparator

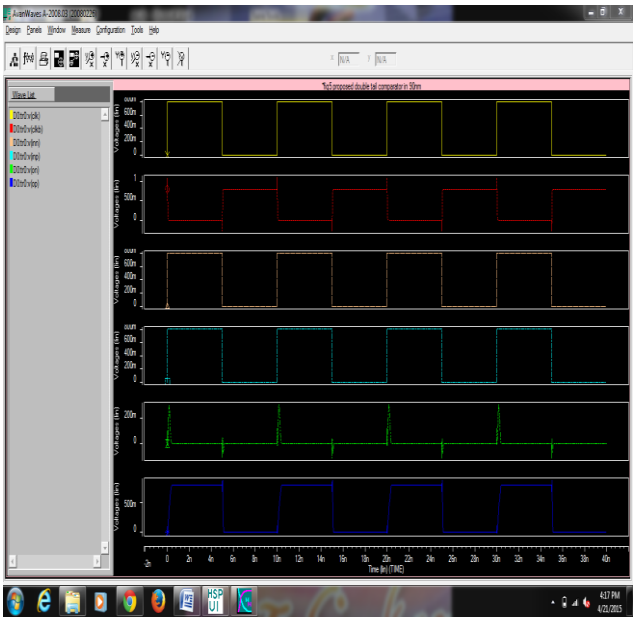

Fig. 8. Waveforms of Proposed double tail comparator

VII. PERFORMANCE COMPARISON

The performance comparison given in table I shows the average power dissipation and delay of all the discussed comparators.

TABLE I
Performance Comparison of Various Comparators

Design	Power (W)	Delay (ps)
Conventional Dynamic Comparator	1.2597E-06	382.22
Conventional double tail comparator	2.1689E-06	369.4
Modified double tail comparator	6.8980E-07	105.62
Proposed double tail comparator	5.6047E-07	91.42

From the table, it is observed that the average power consumption, and the delay of the proposed comparator are significantly reduced.

VIII. CONCLUSION

In this paper, a novel double tail comparator is designed and simulated using 90nm CMOS technology. From the simulated results it is observed that the delay of the proposed double tail comparator is 91.42ps which is comparatively less than the earlier comparators. Also the average power consumption of the proposed double tail comparator is calculated as 0.5604µW. Hence the proposed double-tail dynamic comparator can be used for the design of high speed low power ADCs as the delay and power are reduced and hence resulting in faster operation.

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