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# A 3-6 Ghz Current Reuse Noise Cancelling Low Noise Amplifier For WLAN And WPAN Application

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**ABSTRACT**
A wideband low-noise amplifier (LNA), which is a key block in the design of broadband receivers for multiband multimode wireless communication standards, is presented in this design. A ultra-wideband common gate low noise amplifier (LNA) for 3–6 GHz WLAN and WPAN applications is presented in which consist of three stages. In first stage common gate topology with noise cancelling increases linearity, in second stage is to increase the gain and third stage is buffer is used with output matching. All parameter analyzed in 0.13 µm RF CMOS process with ADS tool.
***Keywords:-*** ADS(Advanced Design system),LNA(low noise amplifier), Noise Cancelling

## I. INTRODUCTION

Wireless communication system is commonly used in our daily life. The emerging of the new wireless communication standards would further push the development of multifunction mobile devices in to market. However, different mobile communication standards are using different modulation and different operation frequencies. RF system is designed for a multifunction device which could work with application that supports various wireless communication standards.

Low noise amplifier is one of the most critical components in RF receiver. In wireless communication system, low noise amplifier is first block in the front end of a radio receiver circuit. The noise figure of the LNA significantly impacts the overall noise performance of the receiver. On the other hand, the power gain of the LNA significantly suppresses noise contributions from subsequent stages, so that it as well impacts the overall noise performance of the receiver. Wireless application are also defined as battery powered devices power consumption is therefore a more concern for the LNA. The baseband output is digitally sampled and handed over to a baseband DSP in order to perform detection and further processing on the received signal. As far as the RF design is concern, however we do not need to know prior information what happen after the digital sampling. All we have to care about is SNR at output of the IQ low pass filter (LPF). Then for a given SNR level the output performance is a function of modulation type, coding scheme etc. which may change dynamically if he radio has multimode function. The received signal entering the antenna is filtered by first band pass filter (BPF) and second BPF (sometimes called preselectors) whose function is essentially protection against various spurious phenomena, mainly far out interferers (many channels away from the desired signal). The low noise amplifier (LNA) contributes to sensitivity, but is not mandatory and may be omitted when an active type first mixer employed. The first mixer converts the incoming signal to IF frequency with the help of local oscillator (LO). Signal often referred to as the injection. In essence the mixer perform the mathematical multiplication of the incoming signals with the injection signal, which ultimately results in subtracting (or summing) the instantaneous injection phase from the instantaneous phase of any carrier reaching the mixer input. If the injection is corrupted by parasitic modulation, as a result of the phase substraction, every incoming signal acquires the very same phase modulation of the LO. Therefore, if a strong interfere reaches the mixer input, it may spread out in to the receive band, generating a serious disturbance. This is all about the receiver section and what is the role of LNA in receiver.

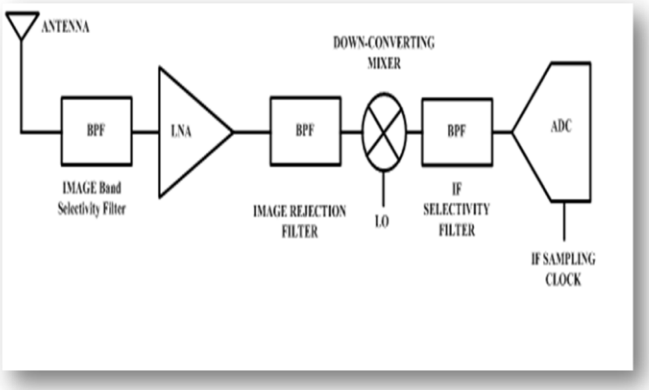


**Fig 1.receiver architecture**

## II. PROPOSED WORK

**First stage:**

As per our requirement in the first stage noise cancelling technique along with linearity improvement technique is used in it. Also their current reused single branch[1,3] will be created so it can take half current than required current. This first stage is also connected to the input matching of the block diagram and output is connected to the second stage.

**Bandwidth enhancement technique**:

The shunt peaking bandwidth enhancement technique is used to flat the gain. This block is connected to the first stage of the circuit.

**Second stage:**

The second stage is gaining stage. To increase gain common source is used in the gaining stage. The output is connected to last stage.

**Bandwidth enhancement technique:**

This also connected to gaining stage of the circuit because we get maximum flat gain in it throught out 3 to 6 GHz frequency. Here shunt double series peaking bandwidth enhancement technique is used in it.

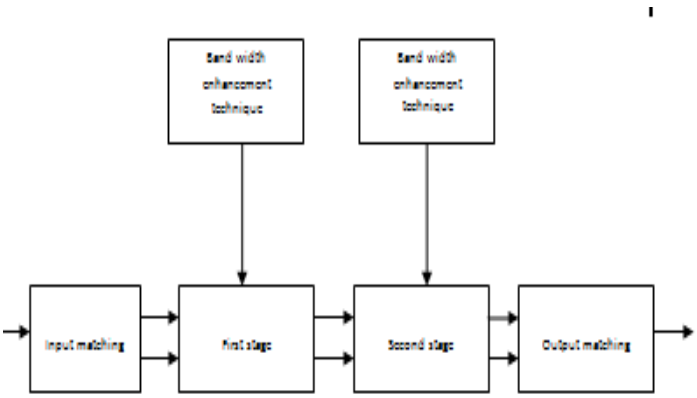


**fig 2. Block diagram**

**Input matching:**

The next step in LNA design consist of noise and input return loss. For the wideband input matching common gate technology [2] is used in it.Input return loss defines how well the circuit is matched to 50 matching of the source impendance and noise matching are critical in LNA design. In input matching, for simultaneous power and noise matching at multiple frequencies, the real part of Zin has matched to 50 and imaginary part of Zin will be zero. Input matching network is difficult to realize with CMOS, so it is considered as off chip to reduce the chip size.

Output matching:

At output stage also there is a 50 resistance can be place in it. When both input and output resistance value should be matching then it gives better result. From such a way that output matching can be done. Output matching not only reduced the chip size but also has good output matching with much less area.

## III. CIRCUIT DIAGRAM

In the circuit diagram input matching can be done by T type because of the maximum transfer of power. Also C5 in the diagram helps to the input matching. M1 is used for the input matching purpose it is a common gate topology is used in it. M2 and M3 is used for the noise cancelling and linearity enhancement technique. Complementary DS technique is used because of that combination of PMOS and NMOS is used. So because of these current can be use less than the original requirement. For the bandwidth enhancement series resistor RL1and inductor L2 is used. L3 is in between M2 and M3 because noise is generated in between them so foe noise cancellation purpose it is used in it. M4 and M5 is used for to increase the gain of the circuit. In second stage also double shunt series bandwidth enhancement technique is used in it. RL2,,L4,L5,L6 these are component that forms the this technique.

M6 is a buffer is used for the output stage it also helps for the output matching with coupling capacitor Cout. C4 and C2 is used the coupling capacitor in the circuit C3 is used as decoupling capacitor in the circuit. Biasing can be done for the to less power dissipation ,to reduce noise figure and enhance the linearity.

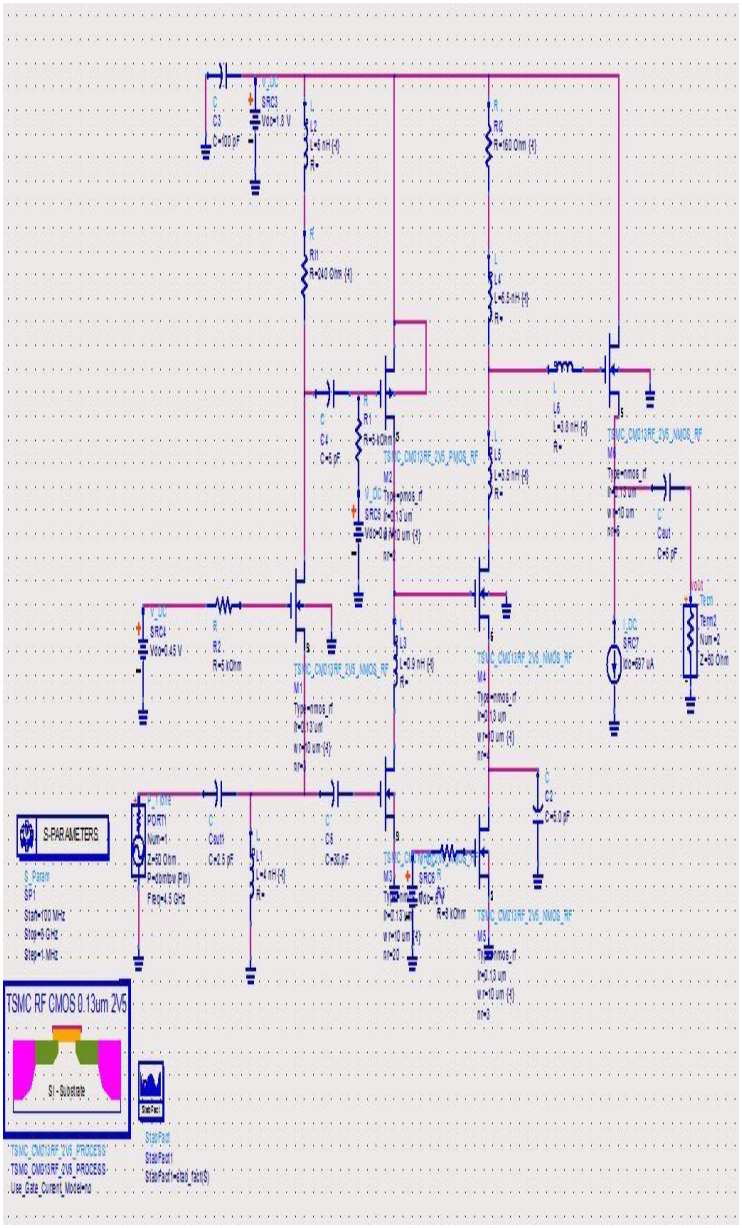


**Fig 3.ciruit diagram**

## IV. LAYOUT

The layout can be done on ads tool. In the layout 6 metal layer is used in it. The inductor is placed on the 6 metal because of high resistivity. Resistor can be formed by polysilicon layer. The capacitor can be formed metal 1 and metal 2. The connection can be formed metal 1 such has inductor to capacitor etc. the gate can be formed by polysilicon layer. For the connection purpose pad can be formed by all metal layer used in it

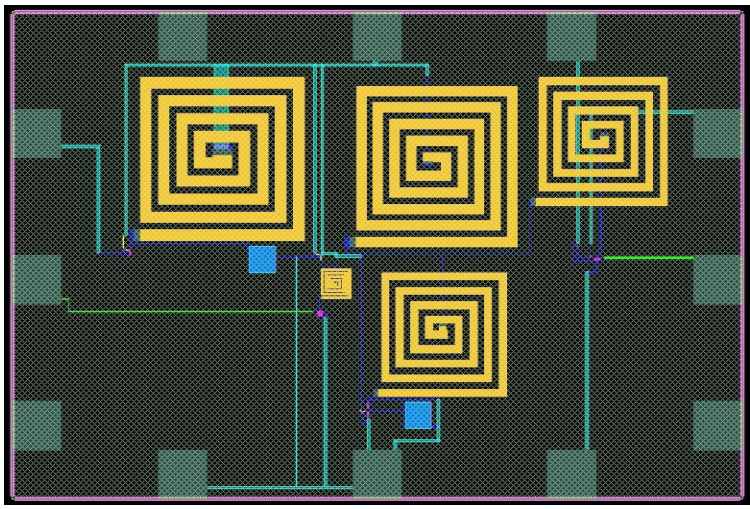

**Fig 4. Layout**

## V. RESULTS

The voltage gain was measured from the SP analysis as the difference in decibels between the output voltage and input voltage. The plot of the voltage gain in Figure shows the voltage gain of the LNA throughout the frequency band of 3 GHz to 6 GHz. The requirement is to get maximum flat gain so according to that voltage gain is at its 21.636 at the start of the frequency band, 3 GHz, and. Small amount it increases the voltage gain reaches 21.651 dB and at 6 GHz

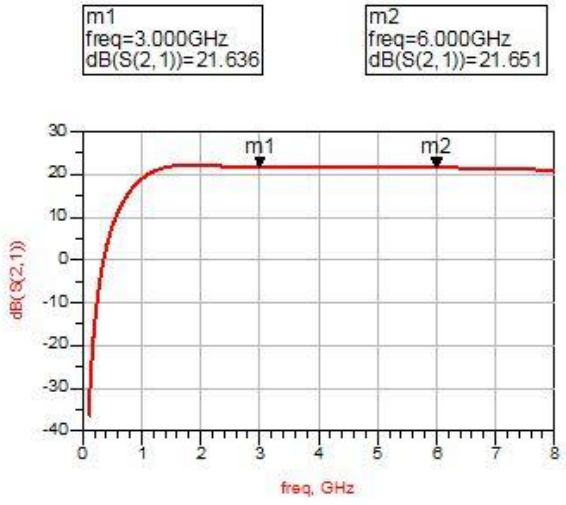


**Fig 5.gain vs frequency**

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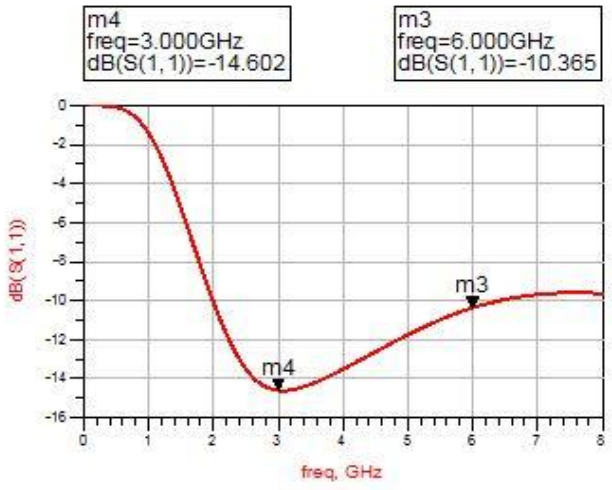


**Fig 6 input return loss vs frequency**

The fig 6 shows input return loss of circuit. The input return loss should be less than 10 dB for better performance. In fig the input matching at 3GHz is -14.602 dB then it can be reduces up to the -10.636 dB at 6 GHz.

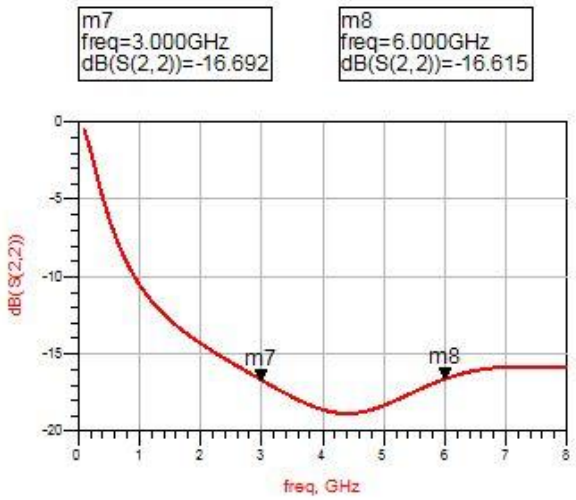


**Fig 7 output return loss vs frequency**

Figure 7shows output return loss. The implemented LNA shows good output matching than the targeted specification. At 3 GHz the output return loss is -16.692dB then some amount it can decreases then it increases up to -16.615dB at 6 GHz.

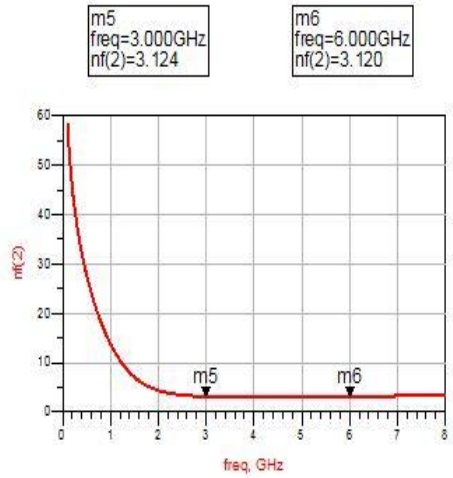


**Fig 8 noise figure vs frequency**

S-parameter analysis was also used to generate the noise figure of the LNA. The noise Figure plot is shown in figure According to specification the noise figure is less than 3.5 dB. The graph shows the noise figure is at 3 GHz is 3.124 dB then it also decreases small amount up to 3.120 dB at 6 GHz.

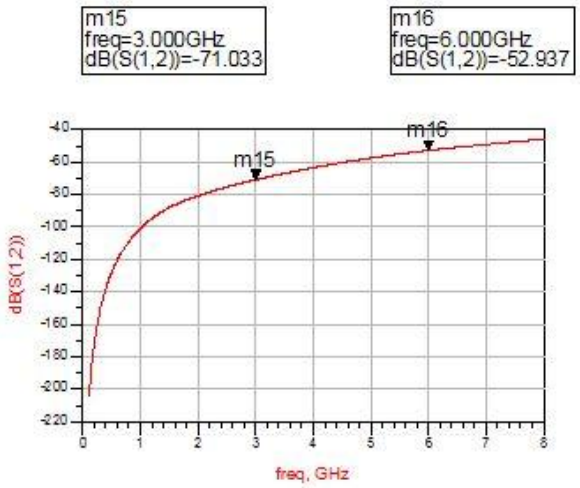


**Fig 9 reverse isolation vs frequency**

Figure 9shows reverse isolation of the implemented LNA which prevent device to damage from signal return back from the next block. The reverse isolation at 3 GHz is -71.033dB then it slowly increases up to -52.967 dB at 6 GHz.

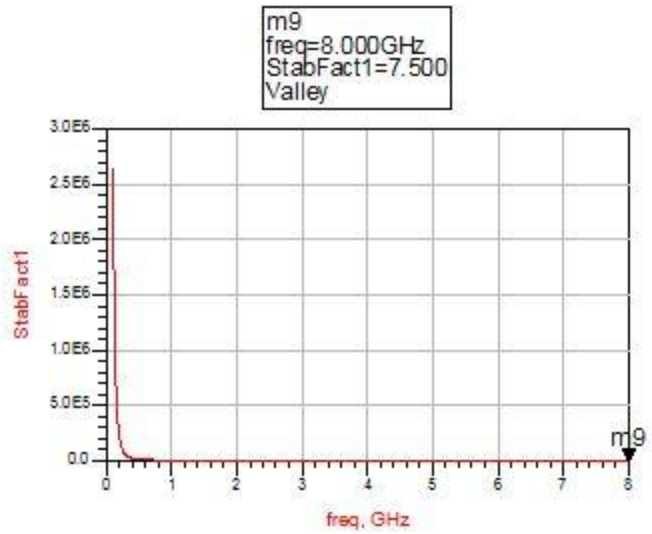


**Fig 10 stability factor vs frequency**

Figure 10 shows stability of an amplifier. It is an important parameter in In band and out of band . the stability factor is always greater than one. The figure stability factor is 7.500 dB.

## VI. CONCLUSION

The implemented amplifier is demonstrated with excellent gain, noise figure and input/output return loss. The simulation result shows that the integrated circuit have met the requirement of LNA. Complete LNA schematic is simulated in Agilent's ADS tool through 0.13 µm CMOS technology.

The proposed common gate LNA topology in this paper uses a new noise canceling technique based on the current reused concept. This approach is based on just one branch complementary structure to cancel the noise of the techniques, which results in lower power consumption. Additionally, it improves the linearity of the first stage and accordingly the total circuit because of its complementary derivative superposition capability

Amplifier is successfully designed achieves a gain of 21.636dB at 3GHz and 21.651dB at 6 GHz. Noise figure is better than 3.5 dB throughout the band. IRL and ORL Input and Output return loss of better than -10dB throughout band is achieved. Power dissipation in the circuit is 11.03 mW at 1.8 voltage supply.

The key issues in the gain, noise and linearity were considered. The LNA was designed to provide gain and to minimize the effect of noise on the AC operation of the circuit.

Finally, layout was performed to examine the physical size of the LNA and its components. During the layout process, the physical sizes of the components were altered to minimize the chip area. Area of 1000um x 700um accommodates all input and output and interstage matching components.

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